TC962

High Current Charge Pump DC-to-DC Converter

Features:

- Pin Compatible With TC7662/ICL7662/SI7661
- High Output Current 80 mA
- No External Diodes Required
- Wide Operating Range 3V to 18V
- Low Output Impedance 28Ω Typ.
- No Low Voltage Terminal Required
- Application Zener On-Chip
- OSC Frequency Doubling Pin Option for Smaller Output Capacitors

Applications:

- Laptop Computers
- Disk Drives
- Process Instrumentation
- μP-Based Controllers

Device Selection Table

Part Number	Package	Operating Temp. Range
TC962COE	16-Pin SOIC Wide	0°C to +70°C
TC962CPA	8-Pin Plastic DIP	0°C to +70°C
TC962EPA	8-Pin Plastic DIP	-40°C to +85°C
TC962IJA	8-Pin CERDIP	-25°C to +85°C
TC962MJA	8-Pin CERDIP	-55°C to +125°C

General Description:

The TC962 is an advanced version of the industry standard TC7662 high voltage DC-to-DC converter. Using improved design techniques and CMOS construction, the TC962 can source as much as 80 mA versus the 7662's 20 mA capability.

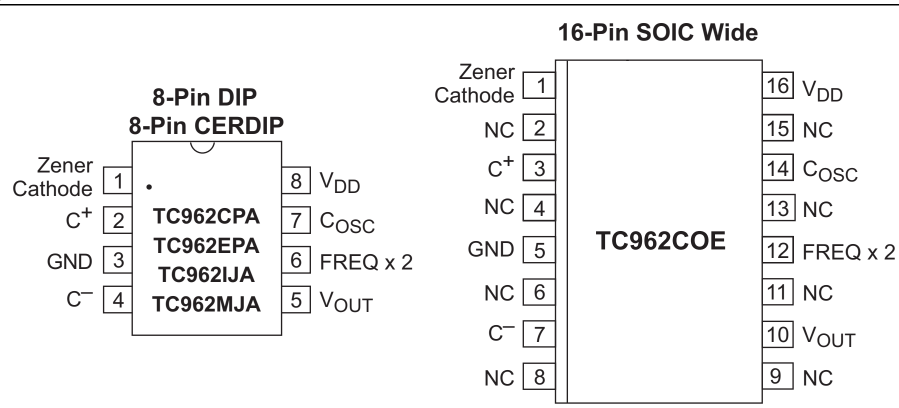
As an inverter, the TC962 can put out voltages as high as 18V and as low as 3V without the need for external diodes. The output impedance of the device is a low 28Ω (with the proper capacitors), voltage conversion efficiency is 99.9%, and power conversion efficiency is 97%.

The low voltage terminal (pin 6) required in some TC7662 applications has been eliminated. Grounding this terminal will double the oscillator frequency from 12 kHz to 24 kHz. This will allow the use of smaller capacitors for the same output current and ripple, in most applications. Only two external capacitors are required for inverter applications. In the event an external clock is needed to drive the TC962 (such as paralleling), driving this pin directly will cause the internal oscillator to sync to the external clock.

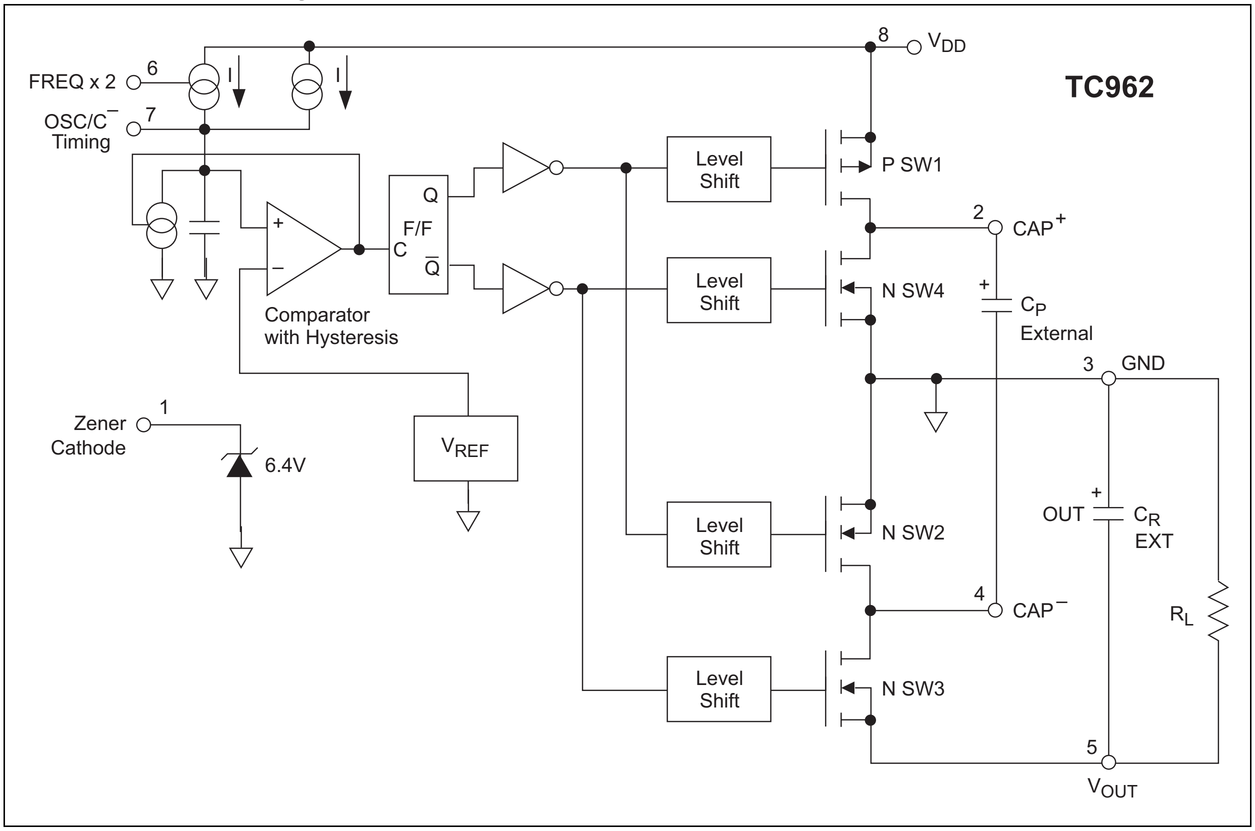
Pin 1, which is used as a test pin on the 7662, is a voltage reference Zener on the TC962. This Zener (6.4V at 5 mA) has a dynamic impedance of 12Ω and is intended for use where the TC962 is supplying current to external regulator circuitry and a reference is needed for the regulator circuit. (See ***Section 3.0 "Applications Information"*** *Applications Information*).

The TC962 is compatible with the LTC1044, SI7661 and ICL7662. It should be used in designs that require greater power and/or less input to output voltage drop. It offers superior performance over the ICL7660S.

Package Type



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage (V_{DD} to GND) ....+18V
Input Voltage Any Pin
.... (V_{DD} +0.3) to (V_{SS} -0.3) **(Note 1)**
Current Into Any Pin..10 mA
ESD Protection ....±2000V
Output Short Circuit .... Continuous (at 5.5V Input)
Package Power Dissipation ($T_A \leq 70°C$)
SOIC ....760 mW
PDIP...730 mW
CERDIP ....800 mW
Package Thermal Resistance
CERDIP, $R\theta_{J-A}$ ....90°C/W
PDIP, $R\theta_{J-A}$ ....140°C/W
Operating Temperature Range
CPA, COE ....0°C to +70°C
IJA...-25°C to +85°C
EPA ....-40°C to +85°C
MJA...-55°C to +125°C
Storage Temperature Range ....-65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC962 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V_{DD} = 15V, T_A = 25°C (See Figure) unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{DD}	Supply Voltage	3	—	18	V	
I_S	Supply Current V_{DD} = 15V V_{DD} = 5V	— — — — — — —	— 510 560 650 190 210 210	— 700 — — — — —	µA	$R_L = \infty$ T_A = +25°C $0 \leq T_A \leq +70°C$ $-55°C \leq T_A \leq +125°C$ T_A = +25°C $0 \leq T_A \leq +70°C$ $-55°C \leq T_A \leq +125°C$
R_O	Output Source Resistance	— — —	32 35 —	37 40 50	Ω	I_L = 20 mA, V_{DD} = 15V I_L = 80 mA, V_{DD} = 15V I_L = 3 mA, V_{DD} = 5V
F_{OSC}	Oscillator Frequency	— —	12 24	— —	kHz	Pin 6 Open Pin 6 GND
P_{EFF}	Power Efficiency	93 —	97 —	— —	%	R_L = 2 kΩ
V_{DEF}	Voltage Efficiency	99 — 96	99.9 — —	— — —	%	$R_L = \infty$ Over temperature range
V_Z	Zener Voltage	6.0	6.2	6.4	V	I_Z = 5 mA
Z_{ZT}	Zener Impedance	—	12	—	Ω	I_L = 2.5 mA to 7.5 mA

Note 1: Connecting any input terminal to voltages greater than V^+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power-up" of the TC962.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin DIP) (8-Pin CERDIP)	Symbol	Description
1	Zener Cathode	Cathode of internal Zener diode.
2	C^+	Positive side of external CP capacitor (pump cap).
3	GND	Ground terminal.
4	C^-	Negative side of external CP capacitor (pump cap).
5	V_{OUT}	Output voltage.
6	FREQ x 2	If grounded, frequency doubles.
7	C_{OSC}	Capacitor to GND will decrease frequency.
8	V_{DD}	Input voltage.

Pin No. (16-Pin SOIC)	Symbol	Description
1	Zener Cathode	Cathode of internal Zener diode.
2	NC	No connect.
3	C^+	Positive side of external CP capacitor (pump cap).
4	NC	No connect.
5	GND	Ground terminal.
6	NC	No connect.
7	C^-	Negative side of external CP capacitor (pump cap).
8	NC	No connect.
9	NC	No connect.
10	V_{OUT}	Output voltage.
11	NC	No connect.
12	FREQ x 2	If grounded, frequency doubles.
13	NC	No connect.
14	C_{OSC}	Capacitor to GND will decrease frequency.
15	NC	No connect.
16	V_{DD}	Input voltage.

3.0 APPLICATIONS INFORMATION

3.1 Theory of Operation

The TC962 is a capacitive pump (sometimes called a switched capacitor circuit), where four MOSFET switches control the charge and discharge of a capacitor.

The functional block diagram shows how the switching action works. SW1 and SW2 are turned on simultaneously, charging C_P to the supply voltage, V_{IN}. This assumes that the on resistance of the MOSFETs in series with the capacitor results in a charging time (3 time constants) that is less than the on time provided by the oscillator frequency as shown:

$$3\ (R_{DS(ON)}\ C_P) < C_P/(0.5\ f_{OSC})$$

In the next cycle, SW1 and SW2 are turned off and after a very short interval of all switches being off (this prevents large currents from occurring due to cross conduction), SW3 and SW4 are turned on. The charge in C_P is then transferred to C_R, *but with the polarity inverted*. In this way, a negative voltage is now derived.

An oscillator supplies pulses to a flip-flop that is then fed to a set of level shifters. These level shifters then drive each set of switches at one-half the oscillator frequency.

The oscillator has two pins that control the frequency of oscillation. Pin 7 can have a capacitor added that is returned to ground. This will lower the frequency of the oscillator by adding capacitance to the timing capacitor internal to the TC962. Grounding pin 6 will turn on a current source and double the frequency. This will double the charge current going into the internal capacitor, as well as any capacitor added to pin 7.

A Zener diode has been added to the TC962 for use as a reference in building external regulators. This Zener runs from pin 1 to ground.

3.2 Latch-Up

All CMOS structures contain a parasitic SCR. Care must be taken to prevent any input from going above or below the supply rail, or latch-up will occur. The result of latch-up is an effective short between V_{DD} and V_{SS}. Unless the power supply input has a current limit, this latch-up phenomena will result in damage to the device. (*See AN763, Latch-up Protection for MOSFET Drivers*.)

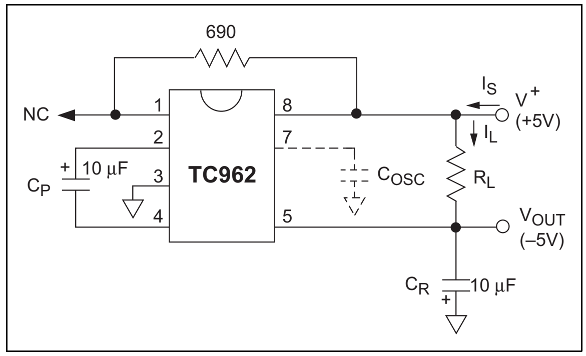


FIGURE 3-1: *Test Circuit*

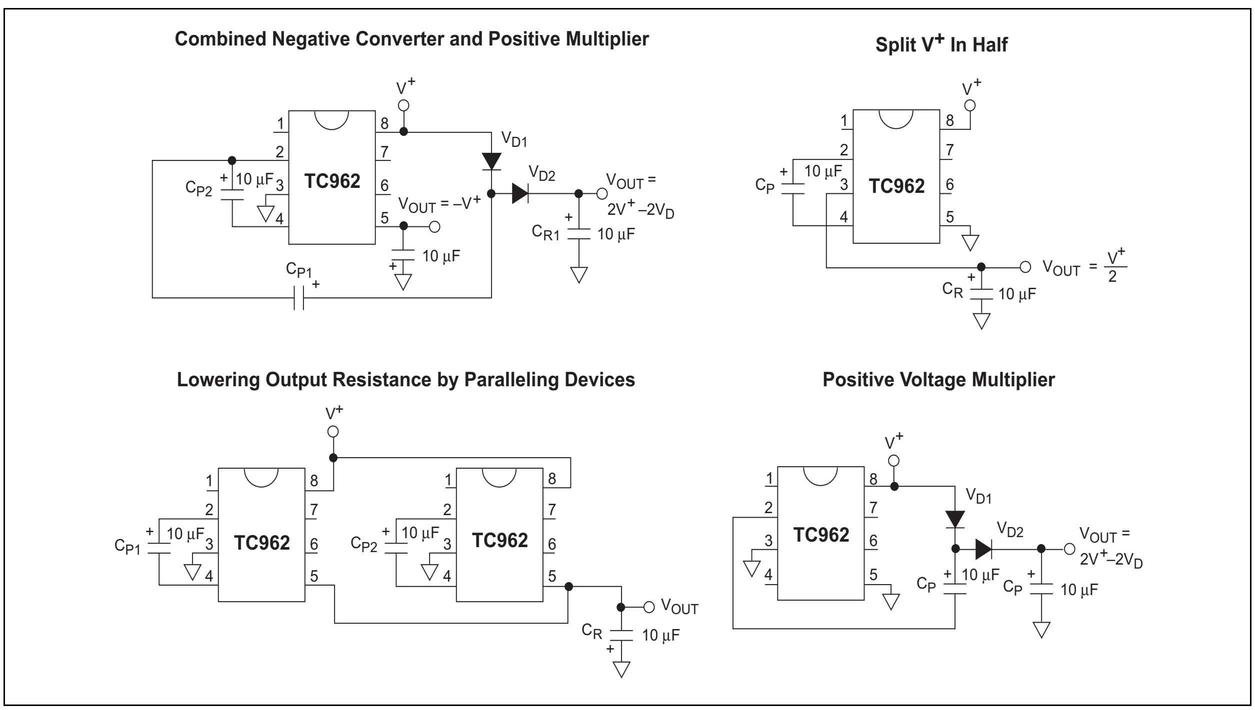


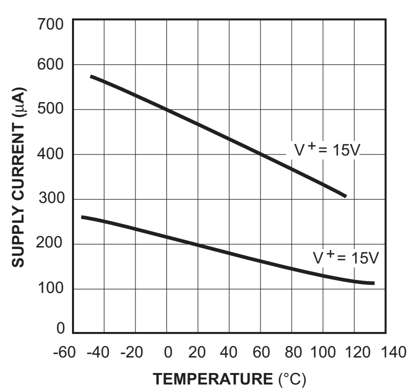
FIGURE 3-2: *Typical Applications*

4.0 TYPICAL CHARACTERISTICS

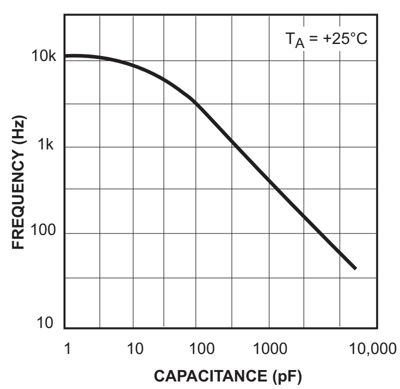
Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Circuit of Figure , $C_P = C_R = 10\ \mu F$, $C_{PESR} \approx C_{RESR} \approx 1\Omega$.

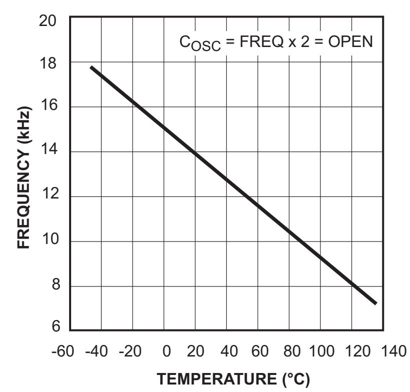
Supply Current vs. Temperature



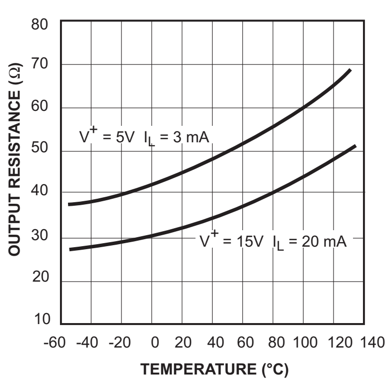
Oscillator Frequency vs. C_{OSC}



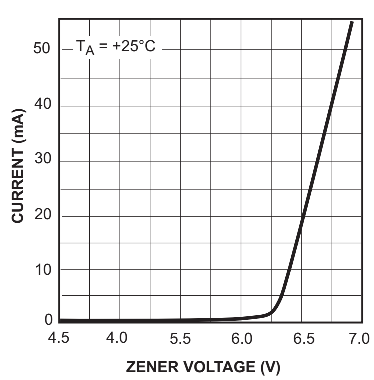
Frequency vs. Temperature



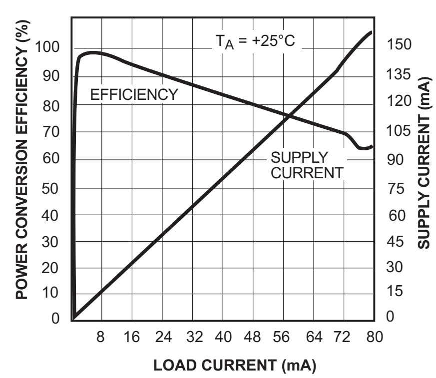
Output Resistance vs. Temperature



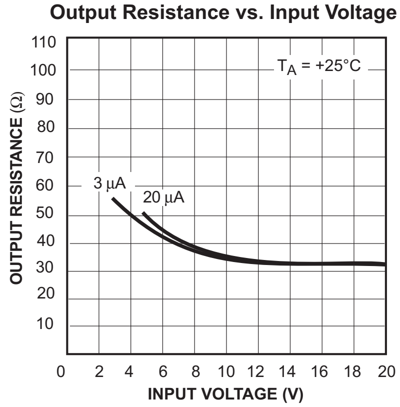
Current vs. Zener Voltage



Power Conversion Efficiency vs. I_{LOAD}



Output Resistance vs. Input Voltage



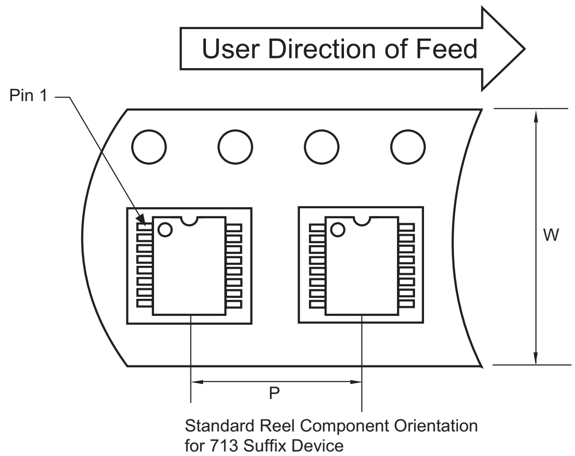
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Package marking data not available at this time.

5.2 Taping Form

Component Taping Orientation for 16-Pin SOIC (Wide) Devices



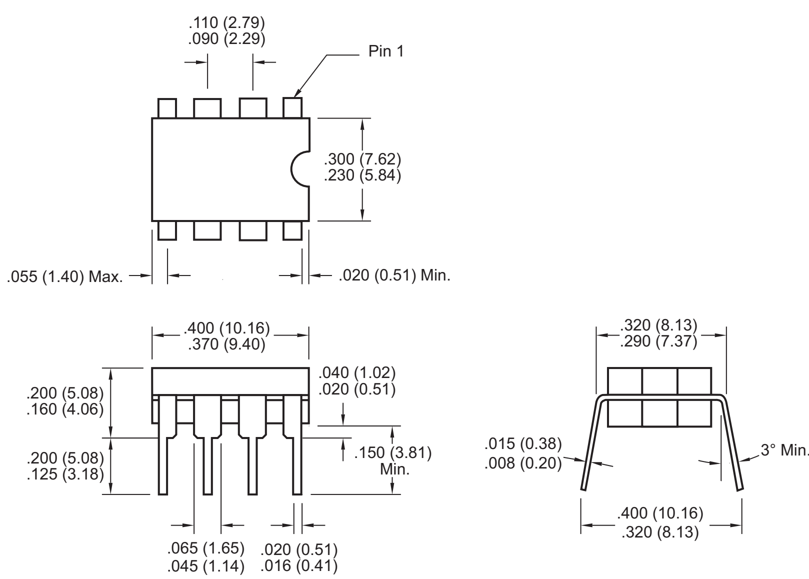
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
16-Pin SOIC (W)	16 mm	12 mm	1000	13 in

5.3 Package Dimensions

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

8-Pin CDIP (Narrow)



Dimensions: inches (mm)

Package Dimensions (Continued)

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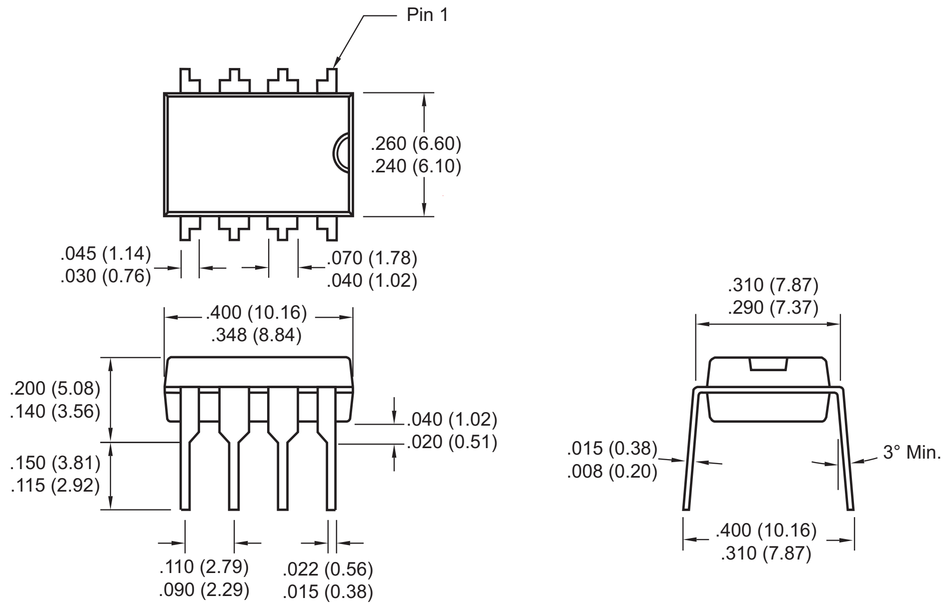
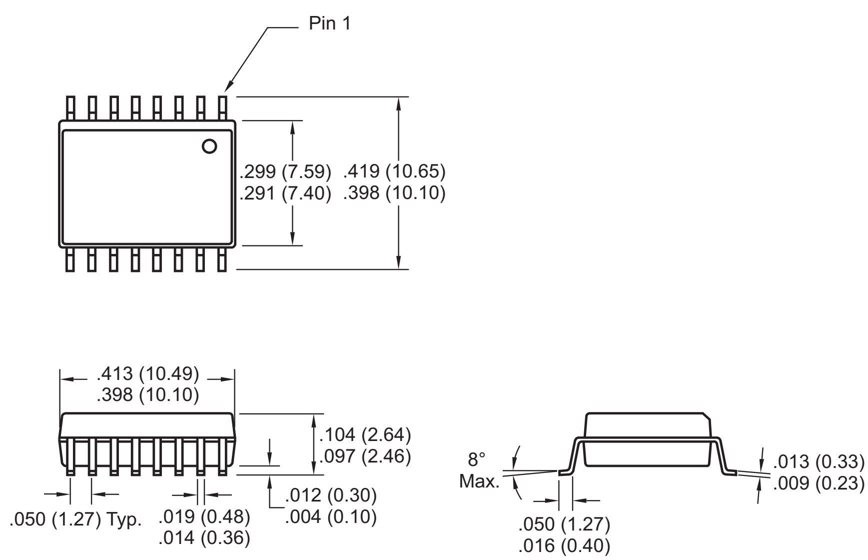
8-Pin Plastic DIP



Dimensions: inches (mm)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

16-Pin SOIC (Wide)



Dimensions: inches (mm)

6.0 REVISION HISTORY

Revision D (December 2012)

Added a note to each package outline drawing.

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